UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,193	07/03/2003	Takashi Takenaka	043034-0180	4129

22428 7590 06/06/2008

FOLEY AND LARDNER LLP
SUITE 500
3000 K STREET NW
WASHINGTON, DC 20007

EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

MAIL DATE	DELIVERY MODE
06/06/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,193	TAKENAKA, TAKASHI	
	Examiner	Art Unit	
	SAIF A. ALHIJA	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,5,9,11,12,15-18 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,9,11,12,15-18 and 21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/3/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4-5, 9, 11-12, 15-18, and 21 have been presented for examination.

Claims 2-3, 6-8, 10, 13-14, and 19-20 have been cancelled.

Response to Arguments

2. Applicant's arguments filed 3 April 2008 have been fully considered but they are not persuasive.

NON-PRIOR ART ARGUMENTS

i) The Examiner is puzzled by Applicants statement on page 9 of their remarks stating:

> to explicitly recite a step that provides a "useful, concrete and tangible" result (claims 13, 14, 16 and 18-20 have been canceled, thereby mooting the rejection of those claims).

The Examiner notes that only claims 13-14 and 19-20 have been cancelled and claims 16 and 18 are still pending.

ii) Applicants argue the 101 rejections of claims 12, and 15-18. Applicants argue that the claims have been amended to recite a useful, concrete, and tangible result. The 101 rejection of claims 15-18 is withdrawn in view of Applicants amendments to the preamble. However the 101 rejection of claim 12 is maintained. The mere comparison of cones does not produce a useful concrete and tangible result since at the very least the mere comparison of cones does not produce a tangible or concrete result. The claim lacks the "means for" or computer readable medium recited in the other independent claims.

iii) Applicant argues the 112 2nd rejections of the claims. The 112 2nd rejections are withdrawn for all claims except claim 21 which does not recite the "logically equivalent" limitation used to overcome the 112 2nd rejections in the other independent claims as well as for antecedent basis issues following Applicants amendments.

PRIOR ART ARGUMENTS

iv) Applicants argue that no comparing of logic cones is performed in Foster so as to determine if an RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones. The Examiner is puzzled by Applicants continued reiteration of equivalent arguments. The Examiner once again asserts that Foster, Blackett, and Lu teach Applicants claimed invention.

With respect to Foster, on page 12, the reference states:

Second, performing equivalence checking early in the design process can help identify complex logic cones while there is still time to restructure the RTL to improve the equivalence checker's overall performance.

Finally, early equivalence checking can identify logic portions that might require alternative solutions for verification, such as logic cones that time out or complex multipliers.

Further on Page 13 Foster states:

ic implementation during synthesis. At this point, equivalence checking is reintroduced automatically to verify consistency between the RTL behavior description and the macrocell instance implementation—simply a self-compare on the RTL module. The reference model and the revised model are contained within the same RTL source. During the equivalence checker's compilation process, we define the `SPECIFICATION` text macro for the reference model and undefine it for the revised model.

By applying the techniques described in this section, we can build an effective RTL equivalence-checking methodology. In the lab at HP,

With respect to Blackett page 70 recites:

fied using simulation. Thereafter, the verified model can serve as a reference against which later revisions can be formally compared by an equivalence checker.

Early in the design process, designers tune their register-transfer level (RTL) models to refine the design's architecture and to produce better synthesis results. Here, an equivalence checker can be used to confirm that changes have not altered circuit behavior.

Once created, a gate-level implementation must be checked for functional equivalence to the higher-level model. This step is necessary even when the implementation has been synthesized, because the synthesis tools and the simulation tools used to check the initial description may not interpret RTL descriptions in the same way.

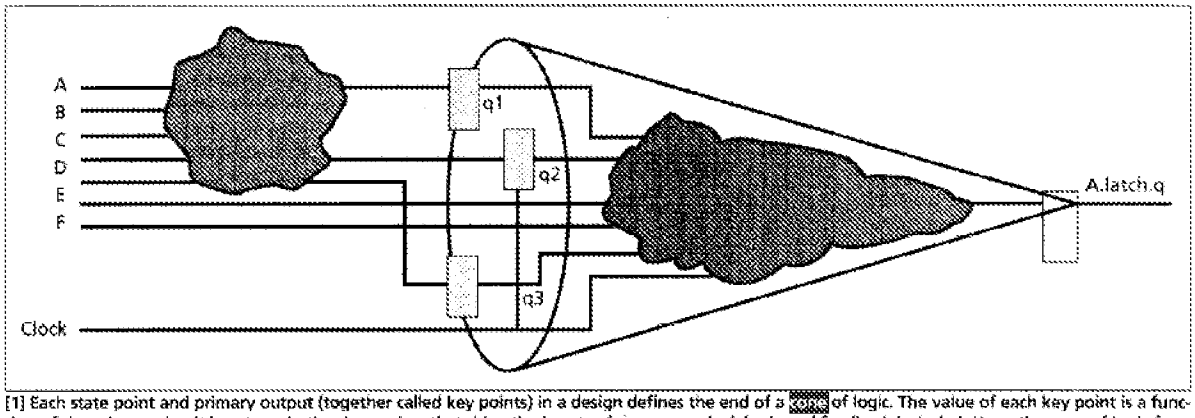
As well as page 68 of Blackett:

Formal verification approaches

Unlike simulation, formal verification requires no vectors. Instead of testing operational scenarios, it relies on mathematical proof that the design being verified and its specification are equivalent. Formal verification tools look at logic function only, not for timing violations or behavior that relies on circuit delays. The tools permit fewer abstractions in the design description than simulation does because they must compile a design's description into a mathematical form, essentially synthesizing the design's behavior into a lower-level representation.

Equivalence checkers use an HDL or netlist description of the engineer's design as the specification with which they compare a revised version, providing conclusive proof that the revision is functionally equivalent to the previous version. As a result,

As well as Figure 1 of Blackett:



[1] Each state point and primary output (together called key points) in a design defines the end of a cone of logic. The value of each key point is a function of the primary circuit inputs and other key points that drive the inputs of the cone—clock logic and feedback included. Here, the cone of logic for a signal A.latch.q has three state point inputs (q1, q2, and q3) and three primary inputs (E, F, and Clock). Its next state is thus a function of these signals.

With respect to Lu, Page 7 recites:

- **Symbolic model checking**

VIS performs symbolic model checking under Büchi fairness constraints [4] which assumes that a system will fairly go to each possible transition state and cannot miss any possible states forever. VIS reports the failure with a counterexample, (i.e., behavior seen in the system that does not satisfy the property). This is called the "debug" trace. Debug traces list a set of states that are on a path to a fair cycle and fail the CTL formula.

- **Equivalence checking**

VIS provides the capability to check the combinational equivalence of two designs. An important usage of combinational equivalence is to provide a sanity check when re-synthesizing portions of a network. VIS also provides the capability to test the sequential equivalence of two designs. Sequential verification is done by building the product finite state machine, and checking whether a state where the values of two corresponding outputs differ, can be reached from the set of initial states of the product machine. If this happens, a debug trace is provided. Both combinational and sequential equivalence verification are implemented using BDD-based routines.

Which leads to, end of page 7,

- **Simulation**

VIS also provides traditional design verification in the form of a cycle-based simulator that uses BDD techniques. Since VIS performs both formal verification and simulation using the same data structures, consistency between them is ensured. VIS can

As well as, page 8,

- **Algorithms**

The fundamental data structure for these algorithms is a multi-level network of latches and combinational gates that is created by flattening the hierarchy. It is assumed that there are no combinational cycles in the network.

The primary inputs and latch outputs are refered to as combinational inputs and the primary outputs and latch inputs are refered to as combinational outputs. The variables of a network are multi-valued, and logic functions over these variables are represented by multi-valued decision diagrams (MDDs) which are an extension of BDDs.

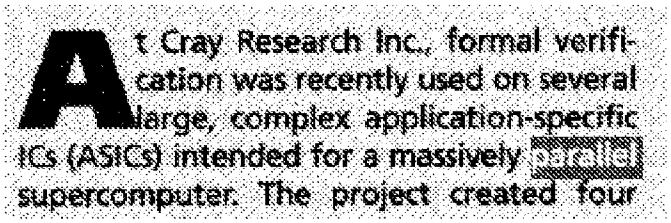
The combinational input variables and next state variables must be ordered before MDDs can be constructed. The combinational input variables are ordered by doing a depth-first traversal of the logic that generates the combinational outputs. The order in which the output logic cones are visited is determined using the algorithm of Aziz et al. [1]. This algorithm orders the latches to decrease a communication complexity bound (where backward edges are more expensive than forward edges) on the latch communication graph. The traversal of an output logic cone is done in such a way that the combinational inputs farthest from the outputs appear earlier in the ordering. Finally, each next state

The indicated sections provided above as well as the previously cited sections of the Foster, Blackett, and Lu references teach Applicants invention. The Examiner notes that Applicants argue means plus function yet provide no specificity as to which embodiments are to be read into the claims and further as per Applicants specification the Examiner is unclear as to how the means plus function, patentable or functionally overcomes the prior art of record which is still anticipatory. Further Applicants argue that the references do not teach the multiple storage means and processing devices recited in claim 21. However,

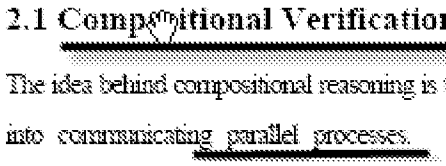
As per Foster see Page 6,

To better understand the technology and mechanics employed in today's equivalence-checking tools, consider a typical computational equivalence model, as shown in Figure 1.

As per Blackett see page 71,


At Cray Research Inc., formal verification was recently used on several large, complex application-specific ICs (ASICs) intended for a massively parallel supercomputer. The project created four

And as per Lu,


2.1 Compositional Verification

The idea behind compositional reasoning is to exploit the natural decomposition of a system into communicating parallel processes.

Following these citations the rejections based on the prior art of record are maintained.

v) Applicants attempt to impart limitations from the specification into the claims, as per page 12 of their remarks, however Applicants use terms such as "may correspond", which is not an explicit definition, and then further request the Examiner to provide a detailed claim mapping. The Examiner has provided a detailed claim mapping in the previous and present office actions. The Examiner asserts that Applicants are arguing storage and data processing means which do not functionally or patentably distinguish the claims from the prior art of record. Applicants have provided no explanation as to how these limitations are functionally or patentably distinct nor have they elaborated on an explicit definition of the terms for which they argue. If Applicants wish to maintain their assertions they are requested to explicitly map their limitations to their specification and explain how they differ functionally and patentably from the prior art of record. For example Applicants argue that the claimed limitation of comparing logic cones to determine logical equivalence differs from Foster, Blackett, and Lu's teaching of equivalence checking and logic cones. The Examiner is puzzled by these arguments since they do not provide any

rationale for their conclusions. The Examiner further notes that the intended use statements argued by Applicants have neither been amended nor adequately addressed. Therefore the rejections are maintained.

vi) Applicants state that the Examiner merely "found three references that describe the use of logic cones, and based on that alone, the Office Action asserts that those references teach or suggest the claimed invention." First the Examiner directs Applicants to 37 CFR 1.3. Second, the Examiner is perplexed by this assertion since the Examiner has provided claim mapping, explanations, and rationale in all the office actions dating back to 25 September 2006.

EXAMINERS NOTE

vii) Examiner has cited particular columns and line numbers in the references applied to the claims for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

viii) The Examiner respectfully requests, in the event the Applicants choose to amend or add new claims, that such claims and their limitations be directly mapped to the specification, which provides support for the subject matter. This will assist in expediting compact prosecution.

ix) Further, the Examiner respectfully encourages Applicants to direct the specificity of their response with regards to this office action to the broadest reasonable interpretation of the claims as presented. This will avoid issues that would delay prosecution such as limitations not explicitly presented in the claims, intended use statements that carry no patentable weight, mere allegations of patentability, and novelty that is not clearly expressed.

x) The Examiner also respectfully requests Applicants, in the event they choose to amend, to supply a clean version of the presented claims in addition to the marked-up copy in order to avoid potential inaccuracies with the version of the claims that would be examined.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 3 April 2008 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

PRIORITY

4. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d).

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02. A process that consists solely of the manipulation of an abstract idea is not concrete or tangibles. See In re Warmerdam, 33 F.3d 1354, 1360, 31 USPQ2d 1754, 1759 (Fed.Cir. 1994). See also Schrader, 22 F.3d at 295, 30 USPQ2d at 1459.

5. **Claim 12 is rejected** under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) The claim recites a method. It should be noted that the claims do not appear to produce a useful, concrete, and tangible result since the claims are directed to merely a comparison of cones. Further, Applicants have not demonstrated how the claims produce a useful, concrete, and tangible result since the claims still recite, in their broadest reasonable interpretation, a comparison of cones.

ii) The claims contain numerous instances of intended use, which are outlined below.

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 21 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

i) Claim 21 recites a determination is made as to whether logic circuits that have been designed… are acceptable to be used. First, it is unclear how a determination is made. Merely stating comparison does not indicate how the comparison is made or what is being compared. Second, it is unclear as to what qualifies as acceptable. Is there an acceptable threshold? Third, it is unclear what mechanism is used to determine acceptability. This renders the claims incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: mechanism to determine acceptability, threshold of comparison, type of comparison, and mechanism for comparison. Fourth, the claim limitations contain numerous intended use statements. These issues render the claims vague and indefinite.

ii) Claim 21 recites the limitations "second storage section" and "second data processing device" in the fourth limitation. There is insufficient antecedent basis for this limitation in the claim.

Appropriate correction is required.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1, 4-5, 9, 11-12, 15-18, and 21 are rejected under 35 U.S.C. 102(a) as being clearly anticipated by **"Applied Boolean Equivalence Verification and RTL Static Sign-Off", Harry Foster, hereafter referred to as Foster.**

8. Claims 1, 4-5, 9, 11-12, 15-18, and 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **"As Good as Gold", Blackett, hereafter referred to as Blackett.**

9. Claims 1, 4-5, 9, 11-12, 15-18, and 21 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **"On the Formal Verification of ATM Switches", Jianping Lu, hereafter referred to as Lu.**

Claim Interpretation. It is noted that the phrases "used to", "used for", "to be used in", "for extracting", "for comparing", "for storing", "for compiling", "for receiving", etc. represent an intended use and are therefore not afforded patentable weight. However the claim limitations are cited assuming Applicants subsequently rectify this issue.

Regarding Claim 1:

The references disclose A logic verification system comprising:

a first logic cone extraction section for extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase;

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references.)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

(Lu. Page 8, Paragraph 3 of Algorithms discusses logic cones)

means for determining based on the first logic cones, whether logic circuits that have been designed in a behavioral synthesis phase are acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

a second logic cone extraction section for extracting second logic cones from an RT level description;

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references.)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

(Lu. Page 8, Paragraph 3 of Algorithms discusses logic cones)

and a logic cone comparison section for comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones;

wherein based on the comparison of the first logic cones and the second logic cones, the determining means determines whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 4:

The references disclose The logic verification system according to claim 1, wherein the first logic cone extraction section includes a symbolic simulation section.

(Foster. Page 10, Column 2 Paragraph 2, "symbolic simulation")

(Blackett. Page 69, "A practical platform", symbolic representation/logic expression)

(Lu. Page 3, Paragraph 3, "symbolic model checking." Page 13, "SMV")

Regarding Claim 5:

The references disclose A logic verification system comprising:

a storage section for storing an object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase,

an RT level description generated from the behavioral level description,

correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair,

and compile information including mapping information between the behavioral level description and the object code;

(The citations below discuss equivalency checking as well as model descriptions)

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

a first logic cone extraction section for extracting first logic cones of variables by

searching a code portion and the variables of the object code corresponding to each fragments of descriptions and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information,

setting initial symbol values in the variables,

performing symbolic simulation from the start to end points of the code portion to produce symbol values when the variable symbolic simulation ends,

and using the symbol values as the first logic cones of the variables;

(Foster. Page 10, Column 2 Paragraph 2, "symbolic simulation")

(Blackett. Page 69, "A practical platform", symbolic representation/logic expression)

(Lu. Page 3, Paragraph 3, "symbolic model checking." Page 13, "SMV")

a second logic cone extraction section for extracting second logic cones each for the signals for each fragments of description of RT level description to be compared which are specified by the correspondence information;

a logic cone comparison section for comparing the first logic cones and the second logic cones for each signals for each of the fragments of descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information;

(The citations below discuss logic cones, as well as equivalency checking)

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

(Lu. Page 8, Paragraph 3 of Algorithms discusses logic cones)

means for determining based on the comparison of the first logic cones and the second logic cones, whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

Regarding Claim 9:

The references disclose A logic verification method comprising the steps of:

extracting first logic cones from a machine-executable object compiled from a behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase;

determining, based on the first logic cones, whether logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the first logic circuits;

extracting second logic cones from an RT level description;

and comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones,

(The citations below discuss logic cones, as well as equivalency checking)

(Foster. Page 7, Equivalence Proof Techniques and BDD Techniques. Page 9, Column 1, Paragraph 2 and Column 2, Paragraph 2. See also indicated sections on the provided references. This applies to all other citations of Foster)

(Blackett. Page 69, Paragraph 1, and A Practical Platform, Paragraph 3-4.)

wherein based on the comparison of the first logic cones and the second logic cones, a determination is made as to whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in the manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

Regarding Claim 11

The references disclose The logic verification method according to claim 9, wherein the first logic cones are extracted by performing symbolic simulation.

(Foster. Page 10, Column 2 Paragraph 2, "symbolic simulation")

(Blackett. Page 69, "A practical platform", symbolic representation/logic expression)

(Lu. Page 3, Paragraph 3, "symbolic model checking." Page 13, "SMV")

Regarding Claim 12

The references disclose A logic verification method comprising the steps of:

inputting an object code compiled from an behavioral level description written in a programming language, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and compile information including mapping information between the behavioral level description and the object code, the object code being used for specification verification by simulation on a CPU in a design phase;

searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison.)

(Blackett, Page 69, Left Column, RTL and gate level information)

(Lu, Page 102, First paragraph, RTL, Behavioral equivalency checking)

setting initial symbol values in the variables;

performing symbolic simulation from the start to end points of the code portion;

determining first logic cones of the variables as symbol values when the variable symbolic simulation ends;

(Foster. Page 10, Column 2 Paragraph 2, "symbolic simulation")

(Blackett, Page 69, Left Column, symbolic signals and logic cones)

(Lu. Page 3, Paragraph 3, "symbolic model checking." Page 13, "SMV")

extracting second logic cones each for the signals for each fragments of RT level description to be compared which are specified by the correspondence information;

and comparing the first logic cones and the second logic cones for each signals for each of the descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information; and

determining, based on the comparing step, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

if the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically

equivalent to the second logic cones.

Regarding Claim 15

The references disclose A computer readable medium embodying a computer program product and comprising code that, when executed causes a computer to perform logic verification, the program product comprising the steps of:

a) extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase;

b) extracting second logic cones from an RT level description; and

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison.)

(Blackett, Page 69, Left Column, RTL and gate level information)

(Lu, Page 102, First paragraph, RTL, Behavioral equivalency checking)

c) comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones.

d) determining, based on the comparison of the first logic cones and the second logic cones, a determination is made as to whether the RT level description that have been designed in the behavioral synthesis phase is acceptable to be used in a manufacturing phase for the logic circuits.

If the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 16

The references disclose The computer readable medium according to claim 15, wherein, in the step a), the first logic cones are extracted by performing symbolic simulation.

(Foster. Page 10, Column 2 Paragraph 2, "symbolic simulation")

(Blackett, Page 69, Left Column, symbolic signals and logic cones)

(Lu. Page 3, Paragraph 3, "symbolic model checking." Page 13, "SMV")

Regarding Claim 17

The references disclose A computer readable medium embodying a computer program product and comprising code that, when executed, causes a computer to perform logic verification, the program product comprising the steps of:

a) storing an object code compiled from an behavioral level description written in a programming language, the object code being used for specification verification by simulation on a CPU in a design phase, an RT level description generated from the behavioral level description, correspondence information which specifies information on pairs of fragments of descriptions to be compared which are included in the behavioral level description and the RT level description and which specifies information on pairs of signals to be compared for each description pair, and compile information including mapping information between the behavioral level description and the object code,

b) extracting first logic cones from a machine-executable object code compiled from a behavioral level description written in a programming language;

c) extracting second logic cones from an RT level description;

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison.)

(Blackett, Page 69, Left Column, RTL and gate level information)

(Lu, Page 102, First paragraph, RTL, Behavioral equivalency checking)

d) comparing the first logic cones and the second logic cones to verify equivalence between the first and second logic cones; and

e) determining, based on the comparison of the first logic cones and the second logic cones, whether the RT level description that has been designed in a behavioral synthesis phase is acceptable in a manufacturing phase for the logic circuits,

f) if the RT level description is determined to be acceptable, manufacturing the logic circuits based on the RT level description,

wherein the RT level description that has been designed in the behavioral synthesis phase is determined to be acceptable to be used in a manufacturing phase for the logic circuits when the first logic cones are logically equivalent to the second logic cones,

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

wherein the step b) comprises the steps of:

b.1) searching a code portion and the variables of the object code corresponding to each fragments of description and each signals of behavioral level description to be compared which are specified by the correspondence information by referencing the compile information;

b.2) setting initial symbol values in the variables;

b.3) performing symbolic simulation from the start to end points of the code portion;

and b.4) determining the first logic cones of the variables as symbol values when the variable symbolic simulation ends.

(Foster. Page 10, Column 2 Paragraph 2, "symbolic simulation")

(Blackett, Page 69, Left Column, symbolic signals and logic cones)

(Lu. Page 3, Paragraph 3, "symbolic model checking." Page 13, "SMV")

Regarding Claim 18

The references disclose The computer readable medium according to claim 17, wherein

the step b) comprises the step of extracting the second logic cones each for the signals for each fragments of RT level description to be compared which are specified by the correspondence information,

and the step c) comprises the step of comparing the first logic cones and the second logic cones for each signals for each of the fragments of descriptions to be compared in the behavioral level description and the RT level description which are specified by the correspondence information.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Regarding Claim 21

The references disclose A logic cone extraction apparatus comprising:

first storage means for storing correspondence information which species logic cone extraction areas within a program;

a first data processing means for compiling an object code from a program description, the object code being used to describe logic circuits in a design phase for the logic circuits;

a second storage means for storing the compiled object code output by the first data processing means, and compile information;

a second data processing means for receiving program code describing logic cones, and for receiving the complied object code and the compile information stored in the second storage section, the second data processing device computing and outputting behavioral level logic cones and RT level logic cones;

and a third storage means for storing the behavioral level logic cones .and RT level logic cones output by the second data processing means;

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison.)

(Blackett, Page 69, Left Column, RTL and gate level information)

(Lu, Page 102, First paragraph, RTL, Behavioral equivalency checking)

and a third data processing means for receiving the behavioral level logic cones and the RT level logic cones stored in the third storage means, the correspondence information stored in the first storage means, and the compile information stored in the second storage means, and for performing logic cone comparisons as a result thereof, and

determining means for determining, based on the comparisons of the logic cones performed by the third data processing means, whether the logic circuits that have been designed in the design phase are acceptable to be used in a manufacturing phase for the logic circuits.

(Foster. Page 10, Column 1, Paragraph 1 and Column 2 Paragraph 2, model comparison. Page 12, Effective equivalence checking methodology and Early Often. Page 13, Combined with RTL recoding to optimize tool performance.)

(Blackett. Page 70, Paragraph 1, and Equivalence checking in use, Paragraph 1-3. Page 71, Equivalence checking at Cray Research)

(Lu. Page 3, Paragraph 3. Page 5, Paragraphs 1-2. Page 8, Paragraph 3. Page 117, Paragraph 1-2 discuss equivalency checking)

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. All Claims are rejected.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to SAIF A. ALHIJA whose telephone number is (571)272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kamini S Shah/

Supervisory Patent Examiner, Art Unit 2128

SAA

June 4, 2008